

FIG. 1

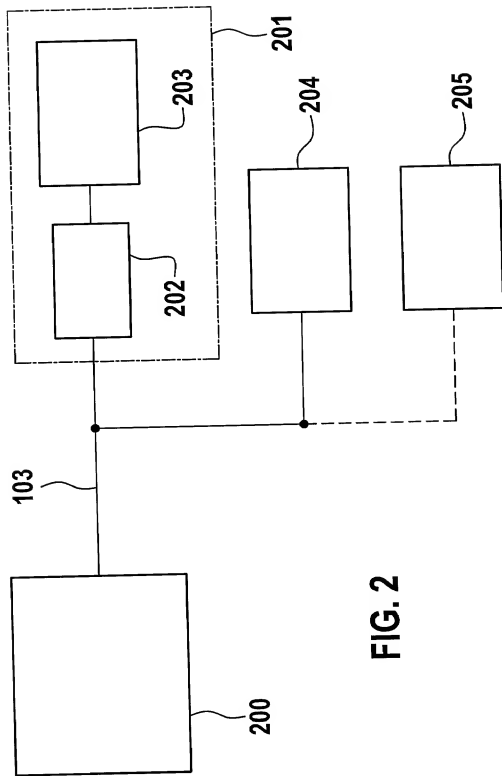


FIG. 2

FIG. 3

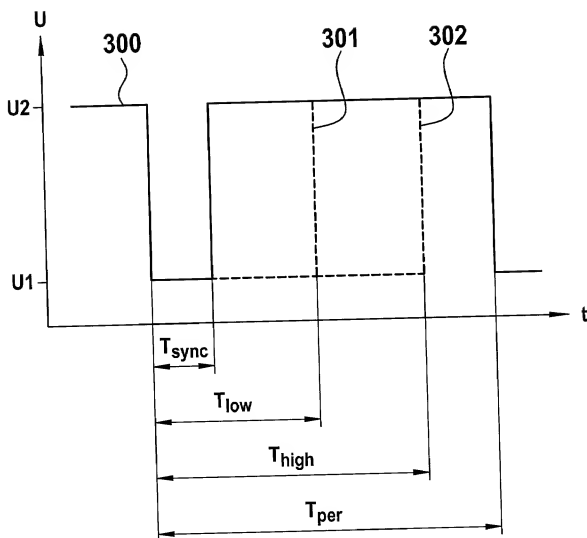
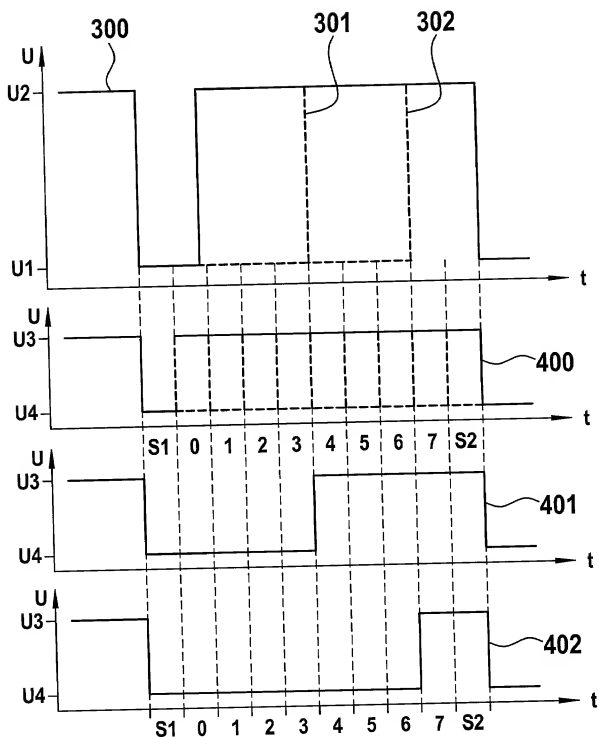


FIG. 4



**FIG. 5**

PWM								
sync	X	1	1	1	1	1	1	1
low	0	0	X	X	1	1	1	1
high	0	0	0	0	0	X	X	X
	0	1	2	3	4	5	6	7